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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,465	06/30/2003	Sau Ching Wong	MLM003US1D	1603
20987	7590	03/09/2006	EXAMINER	
VOLENTINE FRANCO, & WHITT PLLC			HUR, JUNG H	
ONE FREEDOM SQUARE			ART UNIT	
11951 FREEDOM DRIVE SUITE 1260			PAPER NUMBER	
RESTON, VA 20190			2824	

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/611,465

Applicant(s)

WONG, SAU CHING

Examiner

Jung (John) Hur

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 December 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 12-24, 27 and 28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 12-24, 27 and 28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 21 December 2005 has been entered.

Amendment

2. Acknowledgment is made of applicant's Amendment, filed 21 December 2005. The changes and remarks disclosed therein have been considered.

Claims 27 and 28 have been added by Amendment. Therefore, claims 12-24, 27 and 28 are pending in the application.

Interview

3. Acknowledgment is made of personal interview, conducted on 07 February 2006, with Mr. Kenneth Springer and Mr. Ben Westover. See Interview Summary, dated 10 February 2006.

Specification

4. Claims 12 and 14 are objected to because of the following informalities:

In claim 12, lines 11 and 13, "the array plane" is understood as --the array planes-- (plural; see Figs. 4A and 4B).

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In claim 14, line 4, "the read path" is understood as --the read data path--.

Appropriate correction is required.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 12, 18-23, 27 and 28 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-8 of U.S. Patent No. 6,614,685 ("Patent").

Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Regarding claim 12, the claims of Patent recite a flash memory comprising, *inter alia*, a plurality of array planes (see claim 5 of Patent), a plurality of blocks (capable of storing parameters, code and data) of memory cells having a uniform size selected for parameter storage

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(see claim 2 of Patent), memory blocks and spare memory blocks having respective physical addresses (implied by the physical address signal, in claim 5 of Patent), a redundant information block (first and second sets of Flash memory cells, in claim 6 of Patent), a content addressable memory (see claim 5 of Patent), a substitute address memory array (the RAM array, in claims 5 and 6 of Patent), and multiplexing circuitry (see claims 5 of Patent).

Regarding claims 18-23 and 27, Patent claims recite the memory of claim 12 of the instant application, and therefore further recites a related method of operating such memory, comprising, *inter alia*, storing parameters and data (see claim 2 of Patent), storing defect and substitute addresses (claims 5 and 6 of Patent), transferring the defect addresses and substitute address ("loading" in claim 6 of Patent), a second logical address (since, in claim 7 of Patent, the defect and substitute addresses represent block addresses, requiring at least a row address to access the desired memory cells within the selected block), and reading a first array plane while writing to a second array plane (related to simultaneous read and write operations, in claim 5 of Patent).

Patent claim do not disclose storing code. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to store code in a Flash memory, since it was common and well known in the art to store various types of information, including code, parameters and data, in its respective storage blocks of a memory space.

Regarding claim 28, Patent claims recites the method of claim 27, with the exception of the transferring steps (or "loading" in claim 6 of Patent) occurring during a power up. It would

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have been obvious at the time the invention was made to a person having ordinary skill in the art to transfer defect and substitute addresses during a power up, for the purpose of ensuring, as soon as possible upon power up before normal operations, that defective memory blocks are not accessed.

7. Claims 13-16 and 24 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-8 of U.S. Patent No. 6,614,685 ("Patent") in view of Hazen et al. (U.S. Pat. No. 6,088,264).

Regarding claims 13-16 and 24, Patent claims recite the memory and method of claims 12 and 22 of the instant application, and further recites a write data path and a read data path to permit an array plane to conduct a read operation while another array plane conducts a write operation (see claim 5 of Patent), and each array plane comprising at least one of the spare memory blocks (see claim 8 of Patent).

Patent claims do not recite that each of the blocks comprises 4-K word blocks of memory cells that are connected to permit simultaneous erasure of all of the memory cells in the block, erasing a block in the array plane while other array planes read and write operations.

Hazen discloses a Flash memory with a plurality of array planes (partitions) with erase blocks, with an erase circuitry that erases a block in an array plane while other array planes conduct read and write operations (see for example column 2, lines 37-43).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to configure the memory blocks with 4-K word blocks of memory cells, since block erasing was common and well known in the art (as in Hazen) and discovering

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optimum or workable ranges, or an optimum value of a result effective variable (block size) involves only routine skill in the art.

Further, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to erase a block in an array plane while other array planes conduct read and write operations (as in Hazen), for the purpose of increasing the overall speed of Flash memory operations (see for example Hazen column 1, lines 59-64 and column 2, lines 16-23).

8. Claim 17 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-8 of U.S. Patent No. 6,614,685 ("Patent") in view of Hazen et al. (U.S. Pat. No. 6,088,264) as applied to claim 16 above, and further in view of Abedifard et al. (U.S. Pat. No. 6,665,221).

Regarding claim 17, the claims of Patent, in view of Hazen, recite the memory of claim 16 of the instant application, with the exception of a spare global bit line.

Abedifard discloses a spare global bit line (420 in the redundant column 428 in Fig. 5).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to include a spare global bit line, for the purpose of providing additional levels of redundancy and repair capability and therefore further increasing the yield.

Response to Arguments

9. Applicant's arguments with respect to claims 12-24 have been considered but are moot in view of the new ground(s) of rejection, necessitated by Amendment. See rejections above.

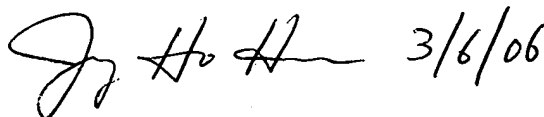
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Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jung (John) Hur
Patent Examiner
Art Unit 2824

jhh